In the Claims

Please cancel claims 1-10 without prejudice.

1-10. (Canceled)

11. (Original) In a cable modem termination system (CMTS) with a plurality of cable interface circuits, each of which includes a cyclical timing counter that provides timing signals to cable modems coupled to each of said interface circuits, a method of synchronizing the timing counter of a first cable interface circuit to the timing counter of a second cable interface circuit comprised of the steps of:

copying a first value of said timing counter of said first cable interface circuit into a storage device;

adding an offset to said first value to create a future timing counter value;

copying said future timing counter value into a storage device;

copying said future timing counter value from said storage device into said timing counter.

12. (Original) The method of claim 11 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of:

a. waiting a predetermined length of time until said timing counter is substantially equal to said future timing counter value;
b. copying said future timing counter value from said storage device into said timing counter.

13. (Original) The method of claim 11 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of:

c. waiting a predetermined length of time until said timing counter increases to a value substantially equal to said future timing counter value;
d. copying said future timing counter value from said storage device into said timing counter.

14. (Original) The method of claim 11 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the step of:

e. triggering the transfer of said future timing counter value from said storage device into said timing counter from a System Controller for said CMTS.

15. (Original) A cable modem termination system (CMTS) with a plurality of interface circuits, each of which includes a cyclical timing counter that provides timing signals to cable modems coupled to each of said interface circuits, said CMTS comprising:

a System Controller means for: copying a first value of said timing counter of said first cable interface circuit into a storage device; adding an offset to said first value to

create a future timing counter value; copying said future timing counter value from said storage device into said timing counter.

16. (Original) The CMTS of claim 15 wherein said System Controller means is a microprocessor.

17. (Original) The CMTS of claim 15 wherein said System Controller means is an application specific integrated circuit

18. (Original) The CMTS of claim 15 wherein said System Controller means is a field programmable gate array (FPGA).

19. (Original) The CMTS of claim 15 wherein said System Controller means is sequential logic.

20. (Original) In a synchronous clock system with a plurality of circuit cards, each of which includes a timing counter that provides timing signals, a method of synchronizing the timing counter of a first circuit card to the timing counter of a second circuit card comprised of the steps of:

copying a first value of said timing counter of said first circuit card into a storage device;

adding an offset to said first value to create a future timing counter value;

copying said future timing counter value from said storage device into said timing counter of said second card.

21. (Original) The method of claim 20 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of:

a. waiting a predetermined length of time until said timing counter of said first circuit card is substantially equal to said future timing counter value;
b. copying said future timing counter value from said storage device into said timing counter of said second card.

22. (Original) The method of claim 20 wherein said step of copying said future timing counter value from said storage device into said timing counter of said second card includes the steps of:

c. waiting a predetermined length of time until said timing counter increases to a value substantially equal to said future timing counter value;
d. copying said future timing counter value from said storage device into said timing counter of said second card.

23. (Original) The method of claim 20 wherein said step of copying said future timing counter value from said storage device into said timing counter of said second card includes the step of:

e. triggering the transfer of said future timing counter value from said storage device into said timing counter from a System Controller for said synchronous clock system.

24. (Original) A synchronous clock system having a plurality of circuit cards, each of which includes a cyclical timing counter that provides timing signals to cable modems coupled to each of said interface circuits, said synchronous clock system comprising:

a System controller means for: copying a first value of said timing counter of said first circuit card into a storage device; adding an offset to said first value to create a future timing counter value; and copying said future timing counter value into a storage device for a second circuit card.

25. (Original) The synchronous clock system of claim 24 wherein said System Controller means is a microprocessor.

26. (Original) The synchronous clock system of claim 24 wherein said System Controller means is an application specific integrated circuit

27. (Original) The synchronous clock system of claim 24 wherein said System Controller means is a field programmable gate array (FPGA).

28. (Original) The synchronous clock system of claim 24 wherein said System Controller means is sequential logic.